AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

1. (currently amended) An apparatus comprising:

a shifter to shift an operand according to an offset parameter, generating a shifted operand and a shift carry operand;

a register coupled to the shifter to store the ~~shifted operand, the register generating a~~ shift carry operand; and

a shift post processor coupled to the shifter and the register to process the shifted operand based on at least a control signal and [[an]] the offset parameter, and comprising a decoder to decode the offset parameter into a mask field, the mask field having a plurality of mask bits, each of the mask bits defining a bit position of the shifted operand to be operated on.

2. (currently amended) The apparatus of claim 1 wherein the shift post processor further comprises:

~~a decoder to decode the offset parameter into a mask field, the mask field having a plurality of mask bits, each of the mask bits defining a bit position of the shifted operand to be operated on; and~~

at least [[a]] one bit formatter coupled to the decoder to format the shifted operand using the control signal and the mask field.

3. (original) The apparatus of claim 1 wherein the control signal is one of a zero extension signal, a sign extension signal, and a use shift carry signal.

4. (original) The apparatus of claim 3 wherein when the mask bit is negated, the corresponding bit in the shifted operand is passed through unmodified.

5. (original) The apparatus of claim 3 wherein when the mask bit is asserted, the corresponding bit in the shifted operand is operated upon according to the control signal.

6. (original) The apparatus of claim 3 wherein the bit formatter comprises:
a gating circuit to gate the control signal using the mask bit; and
a selector circuit coupled to the gating circuit to select one of a bit at the bit position of the shifted operand, the shift carry operand, and a most significant bit of the operand based on the gated control signal.

7. (original) The apparatus of claim 6 wherein the selector circuit selects the bit at the bit position of the shifted operand when the mask bit is negated.

8. (original) The apparatus of claim 6 wherein the selector circuit selects the bit at the bit position of the shifted operand when the mask bit is asserted, the zero extension signal is asserted, the sign extension signal is negated, and the use shift carry signal is negated.

9. (original) The apparatus of claim 6 wherein the selector circuit selects the bit at the bit position of the shift carry operand when the mask bit is asserted and the use shift carry signal is asserted.

10. (original) The apparatus of claim 6 wherein the selector circuit selects the most significant bit when the mask bit is asserted, the zero extension signal and the use shift carry signal are negated, and the sign extension signal is asserted.

11. (currently amended) A method comprising:
shifting an operand <u>according to an offset parameter, generating a shifted operand and a shift carry operand;</u>
storing the ~~shifted operand to generate a~~ shift carry operand; and
processing the shifted operand based on at least a control signal and [[an]] <u>the</u> offset parameter <u>by a processing method comprising decoding the offset parameter into a mask field, the mask field having a plurality of mask bits, each of the mask bits defining a bit position of the shifted operand to be operated on.</u>

12. (currently amended) The method of claim 11 wherein processing the shifted operand further comprises:

~~decoding the offset parameter into a mask field, the mask field having a plurality of mask bits, each of the mask bits defining a bit position of the shifted operand to be operated on; and~~

formatting the shifted operand using the control signal and the mask field.

13. (original) The method of claim 11 wherein the control signal is one of a zero extension signal, a sign extension signal, and a use shift carry signal.

14. (original) The method of claim 13 wherein when the mask bit is negated, the corresponding bit in the shifted operand is passed through unmodified.

15. (original) The method of claim 13 wherein when the mask bit is asserted, the corresponding bit in the shifted operand is operated upon according to the control signal.

16. (original) The method of claim 13 wherein formatting comprises:
gating the control signal using the mask bit; and
selecting one of a bit at the bit position of the shifted operand, the shift carry operand, and a most significant bit of the operand based on the gated control signal.

17. (original) The method of claim 16 wherein selecting comprises selecting the bit at the bit position of the shifted operand when the mask bit is negated.

18. (original) The method of claim 16 wherein selecting comprises selecting the bit at the bit position of the shifted operand when the mask bit is asserted, the zero extension signal is asserted, the sign extension signal is negated, and the use shift carry signal is negated.

19. (original) The method of claim 16 wherein selecting comprises selecting the bit at the bit position of the shift carry operand when the mask bit is asserted and the use shift carry signal is asserted.

20. (original) The method of claim 16 wherein selecting comprises selecting the most significant bit when the mask bit is asserted, the zero extension signal and the use shift carry signal are negated, and the sign extension signal is asserted.

21. (currently amended) A processing unit comprising:

a register file having a plurality of registers, each of the register storing an operand;

an instruction decoder to decode an instruction; and

a shift processing unit coupled to the register file and the instruction decoder to perform an operation on the operand, the shift processing unit comprising:

a shifter to shift an operand according to an offset parameter, generating a shifted operand and a shift carry operand,

a register coupled to the shifter to store the ~~shifted operand, the register generating~~ a shift carry operand, and

a shift post processor coupled to the shifter and the register to process the shifted operand based on at least a control signal and [[an]] the offset parameter, and comprising a decoder to decode the offset parameter into a mask field, the mask field having a plurality of mask bits, each of the mask bits defining a bit position of the shifted operand to be operated on.

22. (currently amended) The processing unit of claim 21 wherein the shift post processor further comprises:

~~a decoder to decode the offset parameter into a mask field, the mask field having a plurality of mask bits, each of the mask bits defining a bit position of the shifted operand to be operated on; and~~

at least [[a]] one bit formatter coupled to the decoder to format the shifted operand using the control signal and the mask field.

23. (original) The processing unit of claim 21 wherein the control signal is one of a zero extension signal, a sign extension signal, and a use shift carry signal.

24. (original) The processing unit of claim 23 wherein when the mask bit is negated, the corresponding bit in the shifted operand is passed through unmodified.

25. (original) The processing unit of claim 23 wherein when the mask bit is asserted, the corresponding bit in the shifted operand is operated upon according to the control signal.

26. (original) The processing unit of claim 23 wherein the bit formatter comprises:
a gating circuit to gate the control signal using the mask bit; and
a selector circuit coupled to the gating circuit to select one of a bit at the bit position of the shifted operand, the shift carry operand, and a most significant bit of the operand based on the gated control signal.

27. (original) The processing unit of claim 26 wherein the selector circuit selects the bit at the bit position of the shifted operand when the mask bit is negated.

28. (original) The processing unit of claim 26 wherein the selector circuit selects the bit at the bit position of the shifted operand when the mask bit is asserted, the zero extension signal is asserted, the sign extension signal is negated, and the use shift carry signal is negated.

29. (original) The processing unit of claim 26 wherein the selector circuit selects the bit at the bit position of the shift carry operand when the mask bit is asserted and the use shift carry signal is asserted.

30. (original) The processing unit of claim 26 wherein the selector circuit selects the most significant bit when the mask bit is asserted, the zero extension signal and the use shift carry signal are negated, and the sign extension signal is asserted.